

Appl. No. 10/267,272  
Amdt. Dated 5/19/2006  
Reply to Office Action of April 19, 2006

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1-5. (Cancelled).

6. (Currently Amended) A circuit, comprising:

a trigger control that adjusts ~~the~~ rise and fall time settings of a clock;

a first register coupled to the trigger control, ~~wherein the first register to~~ contains a default rise and fall settings of the clock, ~~wherein the trigger control uses the rise and fall settings~~ to adjust the clock;

m registers coupled to the first register with "m" being, ~~wherein m is an integer greater than or equal to one, wherein each of the m registers has rise and fall settings that increase a period of the clock, wherein the trigger control accesses the m registers if a power supply voltage is detected to be less than a reference voltage; and~~

n registers coupled to the m registers with "n" being, ~~wherein n is an integer greater than two, the n registers having rise and fall settings that allow the clock to recover the period increases from the m registers and a total decrease in clock period caused by the rise and fall settings of the n registers is less than a frequency guard band.~~

7. (Currently Amended) The circuit of claim 6, ~~further comprising:~~

~~n registers coupled to the m registers, wherein n is an integer great than two, wherein the n registers have rise and fall settings that allow the clock to recover the period increases from the m registers.~~

8. (Cancelled).

9. (Original) The circuit of claim 7, wherein the m registers and the n registers are preset via fuses.

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10. (Original) The circuit of claim 7, wherein the m registers and the n registers are preset via metal options.

11. (Original) The circuit of claim 7, wherein the m registers and the n registers are revised via a TAP controller.

12. (Original) The circuit of claim 7, wherein the m registers and the n registers are revised via a microprocessor status register.

13. (Original) The circuit of claim 7, wherein the m registers and the n registers are revised via a processor abstract layer.

14. (Currently Amended) The circuit of claim 6, further comprising:  
a clock edge control buffer coupled to the trigger control, wherein the clock edge control buffer uses the rise and fall settings provided by the trigger control to independently adjust the clock rise and fall edge timings.

15-17. (Cancelled).

18. (Currently Amended) A method, comprising:  
detecting a droop in a power supply voltage applied to an integrated circuit;  
generating a droop trigger;  
accessing the rise and fall delay values of a clock from a plurality of registers; and  
adjusting the rise and fall edge delays of the clock so that a total reduction of a period of the clock does not exceed a frequency guard band of the integrated circuit.

19. (Original) The method of claim 18, further comprising:  
programming the plurality of registers with rise and fall delay values.

20. (Original) The method of claim 18, wherein adjusting the rise and fall edge delays of the clock comprises stretching the clock period.

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21. (Original) The method of claim 20, wherein adjusting the rise and fall edge delays of the clock comprises recovering delays added to the clock during stretching of the clock period.

22-23. (Cancelled).

24. (New) A circuit comprising:

a first register including a default rise and fall settings of a clock signal;

a first plurality of registers that include a rise and fall settings for increasing a clock period of the clock signal, the first plurality of registers being accessed if a power supply voltage is detected to be less than a reference voltage;

a second plurality of registers that include rise and fall settings for allowing the clock signal to recover the increases of the clock period from the first plurality of registers where a total decrease in the clock period caused by the rise and fall settings of the second plurality of registers being less than a frequency guard band; and

a trigger control in communication with the first register, the trigger control using the rise and fall time settings from the first register and accessing the rise and fall settings of the first plurality of registers if a power supply voltage is detected to be less than the reference voltage.

25. (New) The circuit of claim 24, wherein the first plurality of registers and the second plurality of registers are preset via one of fuses or metal options.

26. (New) The circuit of claim 24, wherein the first plurality of registers and the second plurality of registers are revised via a TAP controller.

27. (New) The circuit of claim 24, wherein the first plurality of registers and the second plurality of registers are revised via a microprocessor status register.

28. (New) The circuit of claim 24, wherein the first plurality of registers and the second plurality of registers are revised via a processor abstract layer.

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29. (New) The circuit of claim 24, further comprising:

a clock edge control buffer coupled to the trigger control, the clock edge control buffer to use the rise and fall settings provided by the trigger control to independently adjust the clock rise and fall edge timings.

30. (New) A method, comprising:

detecting a droop in a power supply voltage;

accessing rise and fall delay values from a plurality of registers; and

adjusting the rise and fall edge delays of a clock signal so that a total reduction of a period of the clock signal does not exceed a frequency guard band of the integrated circuit.

31. (New) The method of claim 30, further comprising:

programming the plurality of registers with rise and fall delay values prior to detecting the droop in the power supply voltage; and

generating a droop trigger signal in response to detecting the droop in the power supply voltage.

32. (New) The method of claim 30, wherein adjusting the rise and fall edge delays of the clock comprises increasing the clock period.

33. (New) The method of claim 30, wherein adjusting the rise and fall edge delays of the clock comprises recovering delays added to the clock signal during increasing of the clock period.

34. (New) A circuit comprising:

a first register including a default rise and fall settings of a clock signal;

a plurality of registers including (1) rise settings to increase a clock period of the clock signal if a power supply voltage is detected to be less than a reference voltage and (2) fall settings to allow the clock signal to recover the increases of the clock period from the first

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plurality of registers where a total decrease in the clock period caused by the rise and fall settings of the second plurality of registers being less than a frequency guard band; and

a trigger control in communication with the first register and the plurality of registers to alter the clock period of the clocking signal.